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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,606	06/27/2003	Kong Weng Lee	70030260-1	2249

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AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
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EXAMINER

HU, SHOUXIANG

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No. 10/608,606	Applicant(s) LEE ET AL.	
	Examiner Shouxiang Hu	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 August 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) 9-11 and 13-18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8, 12 and 19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 12 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakamoto (US 2003/0020126 A1).

Sakamoto discloses a method for fabricating a semiconductor device (Figs. 11A-11D; also see Paragraphs 0011 through 0025), comprising: providing a substantially planar substrate (11) comprising a through-hole formed through drilling and extending between the major surfaces; filling the through-hole inside the substrate with a conductive interconnecting element (TH, through plating); and forming a conductive die mounting pad (14) and a conductive connecting pad (16) on different ones of the major surfaces in electrical contact with the conductive interconnecting element (TH). It is noted that each of the conductive die mounting pad (14) and the conductive connecting pad (16) in Fig. 11C of Sakamoto can be regarded as a pad that has no hole(s) therein. Thus, such a pad without hole(s) therein can only be formed or completely formed after the filling in the thorough hole inside the substrate is completed, regardless whether

portions of the pads may have been formed prior to the filling; otherwise, the filling inside the substrate would not be able to be completed.

Regarding claim 12, the substrate in Sakamoto further comprises an additional filled through-hole (TH) connected to additional conductive bonding pad (15) and conductive connecting pad (17).

Regarding claim 19, the method of Sakamoto naturally further comprises providing a wafer of which the substrate constitutes part; and, after the filling and the forming, singulating the wafer into individual devices, since the method of Sakamoto is for wafer scale chip size packaging (see Paragraphs 10-11).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Kobayashi (US 2003/0040138; of record).

The disclosure of Sakamoto is discussed as applied to claims 1-3, 12 and 19 above.

Although Sakamoto does not expressly disclose that the mounting pad and the connecting pad can be formed through plating on a seed layer, one of ordinary skill in the art would readily recognize that such plating method is commonly used in the art for

forming conductive pads with improved surface contact and/or with low cost, compared with a method of forming the pads entirely with gold and/or with a sputtering method that commonly requires much more expensive equipment than that for plating. It is evidenced in Kobayashi (Figs. 15 and 16), in which, layers 20 and 21 each is readable as a seed layer as the plated portion of gold in the final pads 7-11 are respectively plated thereon. And, the method of Kobayashi further comprises: forming the seed layer (20 and/or 21) on the substrate of an unfired ceramic; firing (i.e., sintering) the ceramic after drilling the hole(s) therein; and forming additional layers (the plated portion, see Paragraph 0016) on the seed layers after the firing.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the gold-coated pad-plating method of Kobayashi into the method of Sakamoto, so that a method for making a semiconductor device with improved surface contact and/or with low cost would be obtained.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Kobayashi, and further in view of Rapoport (US 5,298,687).

The disclosures of Sakamoto and Kobayashi are discussed as applied to claims 1-7, 12 and 19 above.

Although Sakamoto and Kobayashi do not expressly disclose that the seed layer can be formed by screen printing, it is noted that screening printing is one of the art known common methods for forming a patterned seed layer for plating patterned layers with low cost, as evidenced in Rapoport (see the seed layer 2 in Fig. 1), compared to a

method of forming a patterned seed layer through sputtering and/or through photolithography process steps, which both normally require much more sophisticated/expensive sputtering and/or photo machines than that for printing.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the seed-layer screen-printing step of Rapoport into the method collectively taught by Sakamoto and Kobayashi, so that a method for making a semiconductor device with low cost would be obtained.

Response to Arguments

Applicant's arguments filed on July 15, 2005 have been fully considered but they are not persuasive.

Applicant's main arguments include: (A) Sakamoto does not teach to form the pads after the filling; (B) Kobayashi does not teach the recited seedlayer; and (C) There is no teaching or suggestion in the cited references on how to reduce cost.

In response to Argument A above, it is noted that each of the conductive die mounting pad (14) and the conductive connecting pad (16) in Fig. 11C of Sakamoto is interpreted by the examiner as a pad that has no hole(s) therein. Thus, such a pad without hole(s) therein can only be formed or completed formed after completing the filling in the thorough hole inside the substrate, regardless whether portions of the final pads may have been formed prior to the filling; otherwise, the filling inside the substrate would be prematurely blocked by the pads.

Regarding Argument B, the layers 20 and 21 in Kobayashi each naturally functions as a seed layer as the plated portion of gold in the final pads 7-11 are respectively plated thereon, regardless how thick the plated gold layer is.

With respect to Argument C, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, one of ordinary skill in the art readily recognize that forming a conductive pad through plating is commonly cheaper than through sputtering; and that forming a patterned seedlayer through printing is commonly cheaper than through sputtering and/or through photo-patterning, as sputtering and/or photo patterning commonly require much more sophisticated/expensive equipment than plating and/or printing do. And, it would be well within the ordinary skill in the art to incorporate these cheaper methods into the method of making the recited device, so as to form the device with reduced cost. And, applicant's arguments fail to adequately show why such cost reduction would not be desirable to the ordinary skill in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-

Art Unit: 2811


1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH

September 29, 2005



SHOUXIANG HU
PRIMARY EXAMINER